Assessment methodology on mold void defect by scanning acoustic microscopy (SAM) non-destructive Technique

Eric Wong Soon Kiong, Dr. Lai Chin Yung
Failure Analysis Package Development Department
Infineon Technologies Malaysia Sdn Bhd
Malacca, Malaysia
SoonKiong.EricWong@infineon.com

Abstract—Scanning acoustic microscopy (SAM) method with inverted inspection direction has been successfully develop and evaluate the quality of flip chip underfill and interconnect bonds in manufacturing of microelectronic components. Acoustic microscopes utilize high frequency ultrasound transmitting through the silicon chip backside in one scan to access and examine the internal structures in optically opaque materials. These non-destructive methods relatively enable the defect localization which leads microstructural examinations involving destructive analysis sample preparation. For the justification of accuracy of SAM method analysis, a destructive cross-sectioned and mechanical lapping physical analysis were performed for preparing the samples and examine by optical microscope and Scanning Electron Microscope (SEM) for defect verification. Cases studies have been demonstrated that the capabilities of conventional SAM inspection and advantages over other analysis method.

I. INTRODUCTION

In recent years, driven by the trend to lighter, thinner and smaller competitive products, smaller package types particularly flip chip packages have been consolidated with solder bump interconnections is applied extensively in electronic device manufacturing especially in industrial backend assembly house [1]. Flip chip technology is firmly progressing toward smaller packages which leads to smaller bonds and bumps. A flip chip is a chip that mounted on the substrate with the flip chip active site area facing towards the substrate and the bonding feature is a combination of metal, solder bump and metal pads.

In manufacturing quality control of microelectronic components, non-destructive failure analysis methods are critical and reliable techniques for quality control. New acoustic micro imaging techniques have been developed in the area of power semiconductors working non-destructively as substitution of conventional cross-sectional analysis to evaluate the flip chip attach and targeted to be implemented for mass production inspection has been successfully used in assessing the quality of flip chip underfill and interconnect bonds. In particular, scanning acoustic microscopy (SAM) analysis is nowadays rapidly being adopted and satisfying the in-house failure analysis laboratories requirements provides information by detecting and locating defects such as delamination, voids and encapsulates cracking. It has become a powerful and essential tool in the development of wide range of molded packages because it offers non-destructive imaging of microelectronic devices [1-4]. The conventional SAM method works by utilize high frequency ultrasonic energy (typically 10MHz and higher) from a transducer at a small point on a target object to assess the device integrity and characterize material properties and changes. SAM is a suitable tool for detecting and locating defects particularly defects such as pre-existing voids/internal mold void underneath the flip chip active site area are cases of what been observed and has shown promising results [3].

In this study, we evaluate and explain SAM as a tool to examine and investigate the defects in the flip chip interconnects by analysis of the reflection of high frequency ultrasonic pulses. This new idea and method was to inspect and examine the molded flip chip packages in the inverted direction by scanning through the flip chip backside. This new acoustic micro imaging technique has been triggered us to strengthen and utilize the capabilities of SAM by evaluating a method which uses high frequencies of ultrasonic pulses [3].

II. EXPERIMENTAL

ATSLP is a flip chip package normally containing more than 10 copper pillars on the silicon chip active area. The ATSLP flip chip packages have two interfaces such as very short chip substrate interconnection lengths i.e. the flip chip interface to solder bump and the solder bump to the substrate interface (Fig. 1). For conventional scanning acoustic microscopy (SAM) inspection typically uses high frequency ultrasonic energy to detect internal package related failures and defects. The C-SAM (C-Mode Scanning Acoustic Microscope) was used in this study to generate images of samples at specific depth levels typically scanning horizontally across the silicon chip backside to acquire a planar view (C-scan) in one scan. By using this C-SAM transmission acoustic imaging technique the complex flip chip package interface could be assessed and examined more precisely [4].
The thickness of the component package will determine the transducer frequencies been use. Flip chip bonds are relatively small in size and this necessitates evaluation at high imaging resolution in acoustic image in order to assess the small features in the flip chip interconnects. The thinner of the component package, the higher the ultrasonic frequency probe been used leads to higher resolution in the transmission acoustic images [4]. Generally the resolution increases with the increases of ultrasonic frequency, while the penetration depth decreases [3]. In this analysis work, the failure analysis process normally starts evaluated the voiding underneath the silicon chip active area at frequencies from 50MHZ with focal length 1.000inches and 0.146mm spot size.

For the verification of the accuracy of detected failures or defects such as delaminations and voiding underneath the silicon chip active area after performed by C-SAM (C-Mode Scanning Acoustic Microscope), the sample areas with the highest number of defective areas were then subjected to destructive physical analysis i.e. mechanical cross-section polishing and mechanical lapping analysis. The samples that subjected to perform cross-sectioned, polished and finally high resolution imaging was performed by conventional optical microscope and ultra-high resolution scanning electron microscope (SEM) for defects and failures verification [1,7].

A. SAM equipment setup

The conventional SAM is performed in a tank and the samples were immersed in thermostat controlled water at room temperature. The 50MHz frequency transducer was selected to investigate and evaluate the delamination and voiding underneath the flip chip interface to provide a clear signal from the interface of interest. The focal length of the transducer was 1.000 inches, needed for placing the focus inside the interface die/flip chip interface. The optimum C-scan parameter setting shows the location of gate within 0.10-0.25mm to obtain the image of silicon chip backside and the substrate level. The first very positive signal represent the silicon chip interface signal whereas the second positive signal within the gate shows the substrate interface (Fig. 2). In reflective mode, the Time of flight (TOF) refers to the time taken for an acoustic pulse to travel from a single transducer/receiver to the interface of interest and back [8]. The thickness measurement of flip chip packages requires estimating the TOF echoes reflected from the boundaries of a layer [9]. The optimum Time of flight (TOF) applied is approximately 15.20 and the pixel density of 1024x 960 is optimum for this C-scan analysis (Fig. 3). Based on the color mapping after scanning the samples horizontally by C-scan, the non-defective areas which does not containing delamination or voids appear white. Likewise, the defective areas appear yellow or red correspond to the internal void/mold void underneath the flip chip interface. (Fig. 4).

III. RESULTS AND DISCUSSION

The transmission acoustic imaging is valuable to localize defects and assess large samples size by performed SAM C-scans method scanning horizontally through silicon chip backside in one scan and can be implemented for mass production inspection [6,10]. The SAM inspection is performed by array scanning on molded ATSLP flip chip packages in strip form to investigate the flip chip underfill and interconnect bonds. The SAM C-scan image of defects such as delamination and internal voids at the flip chip under fill interface area readily detected. The red features seen in the SAM images correspond to the internal void/mold void underneath the silicon chip active area. In addition, the area with the white appearance shows the silicon chip backside

![Fig. 1. Schematic diagram of flip chip package internal construction.](image1)

![Fig. 2. C-scan showing the location of the gate containing flip chip backside and lead pad substrate.](image2)

![Fig. 3. SAM C-scan parameter setting](image3)

![Fig. 4. Color mapping used for C-scan analysis.](image4)
which does not containing any delamination or voids underneath the flip chip interface (Fig. 5). Waveform verification has been performed compared the area of non-defective vs defective flip chip under fill. At this level the flip chip underfill sites which is non defective area that does not containing any delamination or voids shows a positive signal within the gate whereas the flip chip under fill sites which is defective areas shows a negative signal within the gate containing delamination or voids (Fig. 6&7) [7].

Fig. 5. C-scan images of molded ATSLP flip chip package with 50MHz transducer inspection scanning horizontally across the silicon chip backside.

Fig. 6. Waveform verification of C-scan in area of non defective flip chip underfill.

Fig. 7. Waveform verification of C-scan in area on defective flip chip underfill.

A. Verification by optical microscope and scanning electron microscopy (SEM) inspection

Mechanical cross-section polishing and mechanical lapping analysis have been the techniques for preparing the samples to be examine by optical microscope and scanning electron microscopy (SEM) for correlative analysis [1,7]. The acoustic cross-section of molded ATSLP flip chip packages shows internal void/mold void underneath the silicon chip active site area from the optical imaging and scanning acoustic microscopy (SEM) imaging (Fig. 8&9). The defective flip chip interface that containing voids matches to the position of the samples areas performed by the C-scan scanning method.

Likewise, similar method has been further investigate on singulated ATSLP flip chip packages by similar C-scan scanning method. The C-scan was applied by scan across the silicon chip backside on singulated flip chip packages to assess the flip chip underneath failures and defects. The C-scan image shows no defects such as delaminations or voids detected underneath the silicon chip active site area (Fig. 11). The samples were then subjected to destructive mechanical lapping analysis for the purposes of correlative analysis.

Fig. 8. Cross sectional imaging of defective flip chip underfill area performed by optical microscope.

Fig. 9. Cross sectional imaging of defective flip chip underfill area performed by scanning electron microscope(SEM).

Fig. 10. C-scan image of molded ATSLP flip chip package in singulated form with 50MHz transducer applied by scanning across the silicon chip backside.

The selected singulate flip chip packages then subjected to proceed with the mechanical lapping analysis starting from the flip chip package topside to grind off the silicon chip and then polish until the copper pillar underneath exposed. The optical imaging shows no defects such as delamination or voids exist at the flip chip underfill and interconnect bonds (Fig. 11).
Fig. 11. Optical imaging of mechanical lapping analysis for singulated molded ASTLP flip chip packages starting from package topside.

Simultaneously, the selected singulated flip chip packages also subjected with the mechanical lapping analysis starting from the flip chip package backside to grind off the lead pad substrate and then polish until the copper pillar IMC area exposed. The optical imaging shows no delaminations or voids exist at the flip chip underfill and interconnect bonds (Fig. 12). These examples proven that the confidence level of failure analysis method acquired to localize and detect the internal void/mold void exist underneath the silicon chip active site area. Hence, further cross-sectional preparations or failures analysis method can be avoided [3].

Fig. 12. Optical imaging of mechanical lapping analysis for singulated molded ATSIP flip chip packages starting from package backside.

IV. CONCLUSION

The necessity of non-destructive failure analysis techniques to evaluate flip chip packages in manufacturing quality control of electronic devices in a fast, costs effective, big sample size and automated way area is demanded. With the case studies, we were able to demonstrate the applications and advantages of conventional scanning acoustic microscopy (SAM) over other non-destructive analysis techniques. Large numbers of devices can be inspected and analyzed within reasonable limits. It also turns out to be an effective way provide excellent and promising method of non-destructive characterization of defect localization such as voids under fill the flip chip interface, die attach and delamination in wide range of components.

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