2019 Semiconductor Advanced Packaging Workshop

Organized by
IEEE Electronics Packaging Society, Malaysia Section

Dates & Venues:
24th September 2019 at Eastin Hotel, Penang
or
25th September 2019 at New World Hotel, Petaling Jaya

"Intelligent Digital Convergence for AI and 5G"

by Professor Dr. Madhavan Swaminathan

John Pippin Chair in Microsystems Packaging & Electromagnetics
Director, 3D Systems Packaging Research Center (PRC)
School of Electrical and Computer Engineering, Georgia Tech (GT), USA.

There are two very interesting emerging applications driving the electronics industry namely, artificial intelligence (AI) and Wireless Communication (5G). AI requires memory centric computing meaning that large amounts of data should be moved over short distances while wireless communication requires that data be transmitted over long distances. This apparent diverging requirements from a technology standpoint will need to converge as the next generation of self-driving automobiles, edge computing devices, intelligent computers etc. emerge. Hence, the need for Intelligent Digital Convergence would require major advances in both semiconductor and packaging technologies that lead to high levels of integration. This lecture will focus on some of the packaging technologies being developed to enable Intelligent Digital Convergence.

"Fan-Out Wafer/Panel-Level Packaging & Heterogeneous Integrations (SiPs)"

by Dr. John Lau Hon Shing

Executive Assistant to Chairman, Unimicron Technology Corporation

Fan-out wafer-level packaging (FOWLP) has been getting lots of tractions since TSMC used their InFO to package the application processor for the iPhone 7. In this lecture, emphasis is placed on the fundamentals and latest developments of these areas in the past three years. Their future trends will also be explored.

Because of the drive of Moore's law, SoC (system-on-chip) has been very popular in the past 10+ years. Unfortunately, the end of Moore's law is fast approaching and it is more and more difficult and costly to reduce the feature size (to do the scaling) to make the SoC. Heterogeneous integration contrasts with SoC. Heterogeneous integration uses packaging technology to integrate dissimilar chips, photonic devices, and/or components (side-by-side and/or stack) with different materials and functions, and from different fabless design houses, foundries, wafer sizes, feature sizes and companies into a system or subsystem. System-in-package (SiP) is very similar to heterogeneous integration, except heterogeneous integration is for finer pitches, more inputs/outputs (I/Os), higher density, and higher performance. For the next few years, we will see more implementations of a higher level of heterogeneous integration, whether it is for time-to-market, performance, form factor, power consumption or cost. In this lecture, the introduction, recent advances, and trends in heterogeneous integrations will be presented.

**Please access online for detailed course outline.*

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Mark your calendar and save the date to attend the **2019 Semiconductor Advanced Packaging Workshop** on **24th September 2019 at Eastin Hotel, Penang** or **25th September 2019 at New World Hotel, Petaling Jaya**.

Participants will get a chance to meet and be inspired by two IEEE renowned speakers who will be sharing their expertise in the most recent packaging trends and development of emerging technologies……

Hurry up and **sign up ONLINE today** to enjoy early bird fees!!!
Exclusive privilege for IEEE Members and students

HRDF CLAIMABLE

REGISTRATION DETAILS

I. WORKSHOP VENUE SELECTION		
*Note: Select only **ONE** of the respective venue*		
24th September 2019	EASTIN HOTEL, PENANG	
25th September 2019	NEW WORLD HOTEL, PETALING JAYA	

II. WORKSHOP SCHEDULE	
TIME	**EVENT**
0800 – 0830	Registration
0830 – 1230	Session 1: **Intelligent Digital Convergence for AI and 5G**
1230 - 1330	Lunch
1330 - 1730	Session 2: **Fan-Out Wafer/Panel-Level Packaging and Heterogeneous Integrations (SiPs)**
**Organizer remains the right to change the workshop schedule without prior notice.*	

III. REGISTRATION FEE		
CATEGORIES	EARLY BIRD (Before 15th AUGUST 2019)	NORMAL FEE (After 15th AUGUST 2019)
[ ] IEEE MEMBER	[ ] RM371.00	[ ] RM477.00
[ ] NON IEEE MEMBER	[ ] RM508.80	[ ] RM614.80
[ ] STUDENTS	[ ] RM371.00	[ ] RM477.00

**Register in group of 5 and get the 6th attendee Free-of-charge.*
***Registration fee includes seminar, lunch, coffee breaks, certificate and a copy of the training material.*

REGISTER ONLINE HERE

Click e-registration link for e-registration or scan the QR code below:

Reminder:
Please bring along a copy of printed receipt or show e-receipt during registration on the workshop day.

IV. PAYMENT DETAILS

Participants are strongly encouraged to register and make the payment via the e-registration link provided above. Kindly contact 1300881588 for necessary technical assistance.

Please email Organizer/ IEEE EPS Malaysia through IEMTPAYMENT@gmail.com
(1) For general query on workshop and,
(2) For group registration of 5 participants and above

Registration and Cancellation Policy:
1. Registration transfer is allowed for the same workshop (i.e., same date and location).
2. Registrants who cancel their registration for any reason will receive a partial refund according to the following schedule:
Registrations cancelled more than 30 days before the event will be refunded 80% of the registration fees, no refund less than 30days.

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Become a member of IEEE-EPS Malaysia Section and enjoy big discounts on our future seminars. Here is how to become a member.
1. Membership application info is at: https://www.ieee.org/membership-catalog/productdetail/showProductDetailPage.html?product=MEMEP021
2. Membership benefit: http://www.ieee.org/membership_services/membership/benefits/index.html
3. EPS home page: https://ieee-epsmalaysia.org/

Who should attend: Engineers and managers responsible for advanced packaging development, package design and package quality & reliability are welcomed to join 2019 Semiconductor Advanced Packaging Workshop……