Session 1: Intelligent Digital Convergence for AI and 5G

Abstract:
There are two very interesting emerging applications driving the electronics industry namely, artificial intelligence (AI) and Wireless Communication (5G). AI requires memory centric computing meaning that large amounts of data should be moved over short distances while wireless communication requires that data be transmitted over long distances. This apparent diverging requirements from a technology standpoint will need to converge as the next generation of self-driving automobiles, edge computing devices, intelligent computers etc emerge. Hence, the need for Intelligent Digital Convergence would require major advances in both semiconductor and packaging technologies that lead to high levels of integration. This lecture will focus on some of the packaging technologies being developed to enable Intelligent Digital Convergence.

Course Outline:

[1] System Drivers
- Computing
- Power
- Wireless Communication

[2] Computing
- Artificial Intelligence
- Machine Learning for Design
- Substrate Technologies
  - Interposers
  - Fan Out Wafer Level Packaging
  - Embedding
  - Performance Comparison
- Assembly
  - Fine Pitch Solder
  - Cu-Cu
- Thermal Management

[3] Power
- Data Centers
- Integrated Voltage Regulators
  - 5V/3.3V1.7V:1V & 48V:1V
- Passive Components
  - Magnetics & Dielectrics
  - Embedded Inductors
  - Embedded Capacitors
- Organic Substrates
- 3D Stacking for Automotive

SiC
Thermal Management
[4] Wireless Communication
5G Requirements
RF Front End Modules
Antenna, Filter and Interconnects
Embedded ICs
Beyond 5G (6G)
Antennas, Substrate Integrated Waveguides
Thermal Management
[5] Summary

Speaker Biography:

Madhavan Swaminathan *is the John Pippin Chair in Microsystems Packaging & Electromagnetics in the School of Electrical and Computer Engineering (ECE) and Director of the 3D Systems Packaging Research Center (PRC), GT. He formerly held the position of Founding Director, Center for Co-Design of Chip, Package, System (C3PS), Joseph M. Pettit Professor in Electronics in ECE and Deputy Director of the Packaging Research Center (NSF ERC), GT. Prior to joining GT, he was with IBM working on packaging for supercomputers. He is the author of 500+ refereed technical publications, holds 30 patents, primary author and co-editor of 3 books, founder and co-founder of two start-up companies, and founder of the IEEE Conference Electrical Design of Advanced Packaging and Systems (EDAPS), a premier conference sponsored by the EPS society. He is an IEEE Fellow and has served as the Distinguished Lecturer for the IEEE EMC society. He received his MS/PhD degrees in Electrical Engineering from Syracuse University in 1989 and 1991, respectively.*

Session 2: Fan-Out Wafer/Panel-Level Packaging & Heterogeneous Integrations (SiPs)

Abstract (Part 1: Fan-Out Wafer/Panel-Level Packaging)

Fan-out wafer-level packaging (FOWLP) has been getting lots of tractions since TSMC used their InFO to package the application processor for the iPhone 7. In this lecture, the following topics will be presented and discussed. Emphasis is placed on the fundamentals and latest developments of these areas in the past three years. Their future trends will also be explored.

Course Outline:

[1] Introduction
[2] Formation of Fan-out Wafer-Level Packaging (FOWLP)
FOWLP Chip-first (die face-down)
FOWLP Chip-first (die face-up)
FOWLP Chip-last (RDL-first)

[3] Fabrication of Redistribution Layers (RDLs)
- Polymer and ECD Cu + Etching
- PECVD and Cu damascene + CMP
- Hybrid RDLs

[4] Warpages
- Kinds of Warpages
- Allowable of Warpages

[5] Reliability of FOWLP
- Thermal-Cycling Test
- Thermal-Cycling Simulations
- Drop Test
- Drop Simulations

[6] TSMC InFO
- InFO-PoP for Smartphones
- InFO_AiP for 5G Millimeter Wave
- InFO for HBM (High Bandwidth Memory)

[7] Samsung PLP
- PoP for Smartwatches
- SiP SbS for Smartphones

[8] Formation of Fan-out Panel-Level Packaging (FOPLP)
- PCB + SAP
- PCB + LDI
- PCB + TFT-LCD
- PCB/ABF/SAP + LDI

[9] Wafer vs. Panel
- Application Ranges of FOWLP and FOPLP
- Critical Issues of FOPLP

[10] Fan-Out RDL for High Performance Applications
- STATSChipPac's FOFC-eWLB
- ASE's FOCoS
- MedieTed's FO-RDLs
- Samsung's Si-Less RDL Interposer
- TSMC's InFO_oS

[11] Trends in FOWLP and FOPLP

[12] Summary

Abstract (Part 2: Heterogeneous Integrations (SiPs))

Because of the drive of Moore's law, SoC (system-on-chip) has been very popular in the past 10+ years. Unfortunately, the end of Moore's law is fast approaching and it is more and more difficult and costly to reduce the feature size (to do the scaling) to make the SoC. Heterogeneous integration contrasts with SoC. Heterogeneous integration uses

packaging technology to integrate dissimilar chips, photonic devices, and/or components (side-by-side and/or stack) with different materials and functions, and from different fabless design houses, foundries, wafer sizes, feature sizes and companies into a system or subsystem. System-in-package (SiP) is very similar to heterogeneous integration, except heterogeneous integration is for finer pitches, more inputs/outputs (I/Os), higher density, and higher performance. For the next few years, we will see more implementations of a higher level of heterogeneous integration, whether it is for time-to-market, performance, form factor, power consumption or cost. In this lecture, the introduction, recent advances, and trends in heterogeneous integrations will be presented.

Course Outline:

[1] Introduction
[2] System-on-Chip (SoC)
    A10
    A11
    A12
[3] Heterogeneous Integrations or SiPs
    Definitions
    Classifications
[4] Heterogeneous Integrations vs. SoC
[5] Heterogeneous Integrations on Organic Substrates
    Amkor's Automotive
    ASE/Apple's Smartwatches
    Intel's Knights Landing with HMCs
    Intel/AMD's CPU/GPU on PCB
    Cisco's Chipset on Organic Interposer
    Shinko's i-THOP
    SMT
    Flip Chip on Board
[6] Heterogeneous Integrations on Silicon Substrates (TSV-Interposers)
    SoW (System-on-Wafer)
    CoWoS (Chip-on-Wafer-on-Substrates)
    TSV-Interposers
    Fabrication of TSVs
    Fabrication of RDLs
    Xilinx/TSMC's CoWoS
    NVidia/TSMC's CoWoS-2
[7] Heterogeneous Integrations on Silicon Substrates (TSV-less Interposers, e.g., Bridges)
    Intel's EMIB
    Imec's Bridge
    ITRI's TSH Bridge

[8] Heterogeneous Integrations on Fan-Out RDL Substrates
[9] Heterogeneous Integration of PoP (package-on-package)
    iPhone's Application Processor with Solder Bumped Flip Chip
    Qualcomm's Application Processor with Solder Bumped Flip Chip
    iPhone's Application Processor with TSMC's InFO
    Samsung's Smartwatches with WOPLP
[10] Heterogeneous Integration of Memory Stacks
    Memory Stack with wirebonding
    Memory Stack with Low Temperature Bonding
[11] Heterogeneous Integration of Chip-to-Chip Stacks
    Face-to-Face Bonding with TSVs
    Face-to-Face Bonding without TSVs
[12] Heterogeneous Integration of CIS (CMOS Image Sensor) and Logic Chip
    Sony's CIS and ASIC Bonding with TSV
    Sony's CIS and ASIC Cu-Cu Hybrid Bonding without TSV
    STMicroelectronics's CIS and Logic Bonding
[13] Heterogeneous Integration of LED (light-emitting diode) and TSV-Interposers
    LED and TSV Interposer Bonding
    LED and TSV Interposer Heterogeneous Integration
[14] Heterogeneous Integration of MEMS (microelectromechanical systems) and Logic Chip
    MEMS and TSV Interposer Bonding
    MEMS and Logic Bonding
    Logic Wafer with MEMS and Cap Wafer Bonding
[15] Heterogeneous Integration of VESCL and PD
    Embedded Heterogeneous Integration of VESCL and PD
    Embedded 3D Heterogeneous Integration of VESCL and PD
[16] Trends in Heterogeneous Integrations

Speaker Biography:

***John H. Lau**, Ph.D., P.E., IEEE Fellow, ASME Fellow, IMAPS Fellow.*

He has been a senior technical advisor of ASM since 2014. With more than 39 years of R&D and manufacturing experience in semiconductor packaging, he has published more than 480 peer-reviewed papers, 30 issued and pending US patents, and 20+ textbooks on flip chip technologies, WLCSP, FOWLP, BGA, TSV for 3D integration, advanced MEMS packaging, lead-free solder and manufacturing, reliability of 2D and 3D IC interconnections.